Amendments to the Specification:

Please amend the specification as follows:

Please replace paragraph starting at page 11, line 21, with the following rewritten paragraph:

Intrinsic amorphous silicon layers 4 are formed on the gate insulating layer 3, and heavily- doped n-type amorphous silicon layers 5 are laminated on both side areas of each intrinsic amorphous silicon layer 4. Source layers 7 and drain layers 8 are held in contact with the heavily- doped n-type amorphous silicon layers 45, and the source layers 7 are spaced from the associated drain layers 8, respectively. Transparent pixel electrodes 9 are held in contact with the source layers 97, and the intrinsic amorphous silicon layers 4, tThe source layers 7, the drain layers 8, and the transparent pixel electrodes 9 are covered with a protective dielectric layer 10. The gate insulating layer 3, storage electrode layers 12, and the associated transparent pixel electrodes 9 form in combination storage capacitors coupled to the pixels, respectively.